**(4) Japanese Patent Application Laid-Open No. 59-169125 (1984) and its corresponding United Sates Patent No. 4,525,380**

⑲ 日本国特許庁（JP）　⑪特許出願公開
⑫ 公開特許公報（A）　昭59—169125

⑤Int. Cl.³　識別記号　庁内整理番号　④公開 昭和59年(1984) 9月25日
H 01 L 21/26　6851—5F
21/324　6851—5F
発明の数 1
審査請求 未請求
（全 6 頁）

⑭半導体ウエハーの加熱方法

㉑特　願　昭58—42203
㉒出　願　昭58(1983) 3月16日
⑫発 明 者　荒井徹治
横浜市緑区元石川町6409番地ウシオ電機株式会社内
⑫発 明 者　三村芳樹
横浜市緑区元石川町6409番地ウシオ電機株式会社内
⑪出 願 人　ウシオ電機株式会社
東京都千代田区大手町2丁目6番1号朝日東海ビル19階
⑭代 理 人　弁理士　大井正彦

明　細　書

1. 発明の名称

半導体ウエハーの加熱方法

2. 特許請求の範囲

1）半導体ウエハーの加熱すべき領域及び加熱を必要としない領域の少なくとも一方に膜を設けることにより加熱すべき領域の表面の反射率を加熱を必要としない領域の表面の反射率よりも小さくし、その後半導体ウエハーに閃光を照射して加熱することを特徴とする半導体ウエハーの加熱方法。

2）膜が酸化シリコンより成り、加熱すべき領域上の膜厚が0.06〜0.15μm の範囲内であることを特徴とする特許請求の範囲第1項記載の半導体ウエハーの加熱方法。

3. 発明の詳細な説明

本発明は半導体ウエハーの加熱方法に関するものである。

半導体ウエハー（以下単に「ウエハー」という。）は、集積回路、大規模集積回路などの半導体デバイスを製作する場合における基板として用いられる。このような半導体デバイスの製作においては、その製作プロセス中に目的に応じて種々の加熱工程が必要とされる。この加熱工程としては、例えばイオン注入層の結晶欠陥を回復させるためのアニール工程、ウエハー中に含有せしめた不純物を熱により拡散せしめる熱拡散工程、不純物の活性化のための熱処理工程等があり、このうち例えばアニール工程においては、従来電気炉によりウエハーを加熱する方法が知られている。しかしながら最近素子の高密度化が要求され、不純物分布の微細化が必要とされることから、アニール時における不純物の熱拡散及び再分布を無視することができなくなり、このためアニール時間は短時間であることが要求されるようになつたが、電気炉では短時間加熱が困難である。

これに対して最近レーザビーム或いは電子ビームを用いたアニール方法が開発され、この方法によれば短時間加熱は可能であるが、照射ビームが単一波長であるため、照射ビームの干渉作用が著

しくこれによりウエハー表面に損傷が生ずること、ビームを走査する場合には走査幅の境界部分における不連続性或いは不均一性の問題が生ずること等の問題点を有し、特に大面積のウエハーのアニールには不向きである。

このようなことから、現在閃光放電灯よりの閃光照射によりウエハーをアニールする方法が検討されている。閃光照射によれば短時間で所要の温度に昇温させることが可能であり、しかも閃光は単一波長の光ではないため干渉が生じにくくて損傷が生ぜず、その上、閃光はビームではないため走査する必要がなく従つて走査によつて生ずる走査幅の境界部分における不連続性或いは不均一性の問題点を有さず、大面積のウエハーを加熱することができる等の利点を有している。

しかしながらウエハーの加熱処理においては加熱すべき部分を加熱することが必要であつて、加熱を必要としない部分を加熱することは好ましくないが、例えばアニール工程に付する前のウエハーの表面にはイオン注入層、酸化膜によるイオン注入のためのマスク層など種々の層が形成されていて、通常部分によつて反射率が異なり、このため照射線即ち閃光の照射強度を規定したとしても表面の反射率の差異によつて各部分の到達温度が異なり、この結果必ずしも加熱すべき部分が所定の温度に加熱されるとは限らず加熱を必要としない部分が高温にさらされて損傷する場合がある等の問題がある。

本発明は以上の如き事情に基いてなされたものであつて、ウエハーの加熱すべき領域を選択的に加熱することができて加熱を必要としない領域の過熱を防止することができる半導体ウエハーの加熱方法を提供することを目的とし、その特徴とするところは、半導体ウエハーの加熱すべき領域及び加熱を必要としない領域の少なくとも一方に膜を設けることにより加熱すべき領域の表面の反射率を加熱を必要としない領域の表面の反射率よりも小さくし、その後半導体ウエハーに閃光を照射して加熱する点にある。

以下図面によつて本発明をイオン注入後のウエハーのアニールに適用する場合の一実施例について説明する。

第1図は光源として用いる閃光放電灯の一例を示す説明図であり、1，1は一対の電極、2は封体であつて、例えば寸法の一例を挙げると、アーク長Lは40㎜、封体2の内径D1は8㎜、封体2の外径D2は10㎜である。

第2図は、第1図に示した構成の閃光放電灯の多数を用いて構成した加熱炉の一例を示し、この例においては、9本の閃光放電灯3が互に平行で近接した平面P1及びP2内にそれぞれ5本及び4本宛密に並んでいわばチドリ状に配置され、これにより約50㎜×40㎜の閃光面光源Sが形成されている。4は閃光面光源Sの上方及び側方を覆うよう設けたミラーであり、5は閃光面光源Sから約10㎜程度下方に配置したウエハーを保持する試料台である。尚図示はしないが、この試料台5におけるウエハー保持部にはヒーターが設けられていて、このヒーターによりウエハーが閃光照射による主加熱に先立つて予備的に加熱される。6は試料台5に保持されたウエハーである。

このウエハー6は例えば第3図に示す状態のものである。第3図において、60はシリコン基板、62はシリコン基板60の所定部分にイオン注入するために設けられた酸化シリコンより成るマスク層である。61はシリコン基板60の所定部分にヒ素が、エネルギー40keV、粒子数$5\times10^{15}$個/$cm^2$でイオン注入されたイオン注入層である。シリコン基板60の厚さは約300〜650μmであり、イオン注入層61における結晶欠陥部分の深さは約0.2〜1.0μm程度であり、マスク層62の厚さは約0.9μmである。このウエハー6においては、イオン注入層61が加熱すべき領域であり、このイオン注入層61を除いた他の領域が加熱を必要としない領域である。

本発明の一実施例においては、上述の構成の加熱炉を用いて上述のウエハー6に対し次のようにしてウエハー6を加熱してアニールを行なう。

即ち、先ず第4図に示すようにウエハー6の表面全体に厚さ約0.1μmの酸化シリコンより成る薄

７を設ける。この膜７を形成する方法としては従来公知の薄膜製造方法を用いることができる。

次に膜７を設けたウエハー６を第２図に示した加熱炉における試料台５のウエハー保持部に保持せしめ、閃光照射に先立つて試料台５のヒーターによりウエハー６を温度約３５０℃程度にまで予備的に加熱する。

ウエハー６の温度が約３５０℃程度となつた時点において閃光放電光源Ｓによりウエハー６の表面全体に閃光を照射してウエハー６を加熱する。この閃光照射においては、ウエハー６の表面における照射強度は１８.５ジュール/$cm^2$、照射時間（閃光の$\frac{1}{2}$波高長におけるパルス時間幅をいう）は４００マイクロ秒の条件とされる。

以上のような方法でウエハー６の加熱を行なうわけであるが、一般に閃光照射によるウエハーの加熱においては、閃光照射条件とウエハーの物性とによりウエハーの表面の到達温度が理論的に導き出されることが知られている。即ち平均反射率Ｒを有するウエハーに、閃光の$\frac{1}{2}$波高長におけるパルス時間幅ｔ（マイクロ秒）及びウエハーの表面における照射強度Ｅ（ジュール/$cm^2$）の閃光を照射すると、パルス時間幅ｔが略５０マイクロ秒以上である場合には、ウエハーの表面の到達温度Ｔ(℃)は近似的に下記式(1)で表わされる。

$$T = a \cdot (1-R) \cdot E \cdot t^b + T_A \cdots\cdots\cdots\cdots (1)$$

この式(1)において、ａ及びｂはウエハーを構成する物質の熱伝導率、密度、比熱等によつて定まる定数であり、ウエハーがシリコンより成る場合には、ａは約５４０、ｂは約−0.３７である。(１−Ｒ)・Ｅはウエハーに吸収された単位面積当たりのエネルギーである。$T_A$は予備加熱した場合の予備加熱温度である。平均反射率Ｒは下記式(2)によつて定義されるものである。

$$R = \frac{\int I(\lambda) R(\lambda) d\lambda}{\int I(\lambda) d\lambda} \cdots\cdots\cdots\cdots (2)$$

この式(2)において、Ｉ(λ)は波長λにおける閃光強度を表わし、Ｒ(λ)は波長λにおける反射率を表わす。ウエハー加熱用の閃光の場合にはＩ(λ)は略一定であり、Ｒ(λ)は、ウエハーの光学定数（屈折率、消衰係数等）、ウエハーの表面に膜がある場合にはその膜の光学定数（屈折率、消衰係数等）及び膜の厚さにより定められる。

第５図は、ウエハーがシリコンより成り、このウエハーの表面上に酸化シリコン膜を設けた場合の酸化シリコン膜の厚さと平均反射率Ｒとの関係を示す曲線図であり、この図から明らかなように酸化シリコン膜の厚さが約0.0６〜0.１５μmの範囲内では平均反射率Ｒが比較的小さく、厚さが0.１５μm以上では厚さが変わつても平均反射率Ｒはあまり変動せず略0.３１である。

このような理論的背景のもとにおいて、上記実施例の方法によれば、ウエハー６の加熱すべき領域即ちイオン注入層６１の表面には厚さ0.１μmの酸化シリコンより成る膜７が設けられているため、第５図の曲線図から求められるように、加熱すべき領域の表面の反射率が約0.２６となる。一方加熱を必要としない領域即ちマスク層６２が設けられている領域においては、マスク層６２が酸化シリコンより成りその厚さが0.９μmであり、さらにこのマスク層６２上には厚さ0.１μmの酸化シリコンより成る膜７が設けられているのでこの領域における酸化シリコンの厚さは合計1.０μmとなり、同じく第５図の曲線図から求められるように、加熱を必要としない領域の表面の反射率が約0.３１となる。従つて加熱すべき領域の表面の反射率が加熱を必要としない領域の表面の反射率よりも小さくなり、この結果前記式(1)から理解されるように加熱すべき領域の到達温度が加熱を必要としない領域の到達温度よりも高くなり、加熱すべき領域を選択的に加熱することができると共に、加熱を必要としない領域の過熱を防止することができ、結局ウエハーの良好なアニールを達成することができると共にウエハーの過熱による損傷を防止することができる。

因みに、上記実施例におけるウエハー６の表面の到達温度を前記式(1)に基いて計算すると、加熱すべき領域の到達温度Ｔ１は、

$$T1 = 540 \times (1-0.26) \times 18.5 \times 400^{-0.37} + 350 = 1155 (℃)$$

加熱を必要としない領域の到達温度T2は、

$T2 = 540 \times (1-031) \times 18.5 \times 400^{-0.37} + 350 = 1101\ (℃)$

となり、良好なアニールを達成することができしかも加熱を必要としない領域の過熱を防止することができ、実際に加熱処理後において加熱を必要としない領域を調べたところ損傷はみられなかつた。

一方比較テストとして膜7を設けない他は上記実施例と同様にして加熱を行なつたところ、イオン注入層61は露出しており、このイオン注入層61の反射率は0.43と大きく、加熱すべき領域の到達温度T1は

$T1 = 540 \times (1-0.43) \times 18.5 \times 400^{-0.37} + 350 = 970\ (℃)$

加熱を必要としない領域の到達温度T2は

$T2 = 540 \times (1-031) \times 185 \times 400^{-0.37} + 350 = 1101\ (℃)$

となり、加熱すべき領域の到達温度T1が加熱を必要としない領域の到達温度T2よりも低くなつて良好なアニールを達成することができなかつた。

これに対して、閃光面光源Sを調整して照射強度Eを24ジユール/$cm^2$に高くした他は上述の比較テストと同様にして加熱を行なつたところ、加熱すべき領域の到達温度T1は

$T1 = 540 \times (1-0.43) \times 24 \times 400^{-0.37} + 350 = 1155\ (℃)$

加熱を必要としない領域の到達温度T2は

$T2 = 540 \times (1-0.31) \times 24 \times 400^{-0.37} + 350 = 1324\ (℃)$

となり、イオン注入層61のアニールは行なうことができたが、加熱を必要としない領域が大幅に過熱されて新たな結晶欠陥、クラツクなどの損傷が発生しウエハーは実用に供し得ないものとなつた。

以上の実施例によれば次のような効果を併せて得ることができる。即ち、ウエハーとして、シリコンより成り加熱を必要としない領域上に厚さ0.9μmの酸化シリコンより成るマスク層62が設けられているものを用い、膜7の材質として酸化シリコンを選択し、その厚さを0.06〜0.15μmの範囲内即ち0.1μmとしてこの膜7をウエハーの表面全体に設けるようにしているので、第5図に示した曲線図からも理解されるように、加熱すべき領域の表面の反射率が加熱を必要としない領域の表面の反射率よりも小さくなるので、膜7の形成において膜7をウエハーの特定部分に選択的に設けることが不要となるので、膜7の形成作業が極めて容易となる。そして閃光照射に先立つてウエハーを予備的に加熱しているので必要とされる閃光の照射強度を小さくすることができて閃光放電灯の使用寿命を長くすることができる。

以上本発明の一実施例について説明したが本発明においては種々変更が可能である。例えば膜7の材質としては、酸化シリコンの他、窒化シリコン（$Si_3N_4$等）、PSG（$P_2O_5$を8％含有する$SiO_2$より成るガラス）、アルミニウム等を用いてもよく、この場合にも酸化シリコンの場合と同様に膜厚の変化を利用して反射率を変えることができる。そして膜7はウエハーの加熱すべき領域上にのみ設けてもよいし、加熱を必要としない領域上にのみ設けるようにしてもよいし、或いは加熱すべき領域と加熱を必要としない領域の両者にそれぞれ異なる厚さのものを設けてもよく、何れの場合においても膜7を設けることにより加熱すべき領域の表面の反射率が加熱を必要としない領域の表面の反射率よりも小さくなることが必要である。

以上本発明の一実施例をウエハーのイオン注入層をアニールする場合の一例について説明したが、本発明方法は、ウエハーの他の加熱処理においても適用することができる。

以上のように本発明は、半導体ウエハーの加熱すべき領域及び加熱を必要としない領域の少なくとも一方に膜を設けることにより加熱すべき領域の表面の反射率を加熱を必要としない領域の表面の反射率よりも小さくし、その後半導体ウエハーに閃光を照射して加熱することを特徴とする半導体ウエハーの加熱方法であるから、ウエハーの加熱すべき領域を選択的に加熱することができて加熱を必要としない領域の過熱を防止することができる半導体ウエハーの加熱方法を提供することができる。

4.図面の簡単な説明

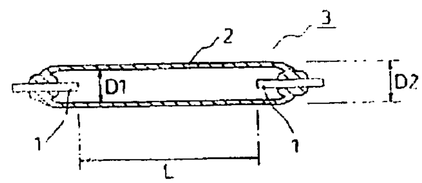
第1図は閃光放電灯の一例を示す説明用断面図、

第2図は閃光放電灯を用いた加熱炉の一例を示す説明用断面図、第3図はウエハーの一例を示す説明用断面図、第4図はウエハーの表面に膜を設けた状態を示す説明用断面図、第5図は酸化シリコンの膜厚と平均反射率との関係を示す曲線図である。

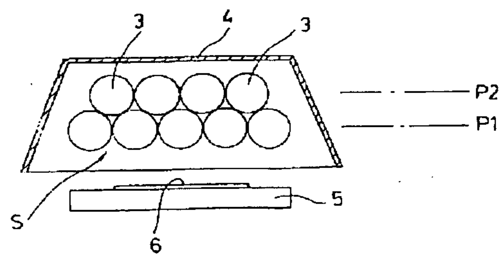
| | |
|---|---|
| 1…電極 | 2…封体 |
| 3…閃光放電灯 | S…閃光面光源 |
| 4…ミラー | 5…試料台 |
| 6…ウエハー | 60…シリコン基板 |
| 61…イオン注入層 | 62…マスク層 |
| 7…膜 | |

代理人　弁理士　大　井　正　彦

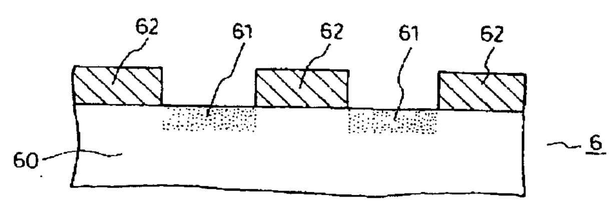
第1図



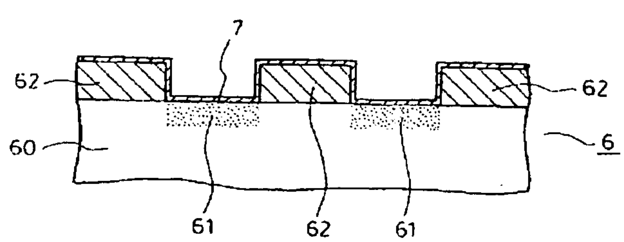

第2図



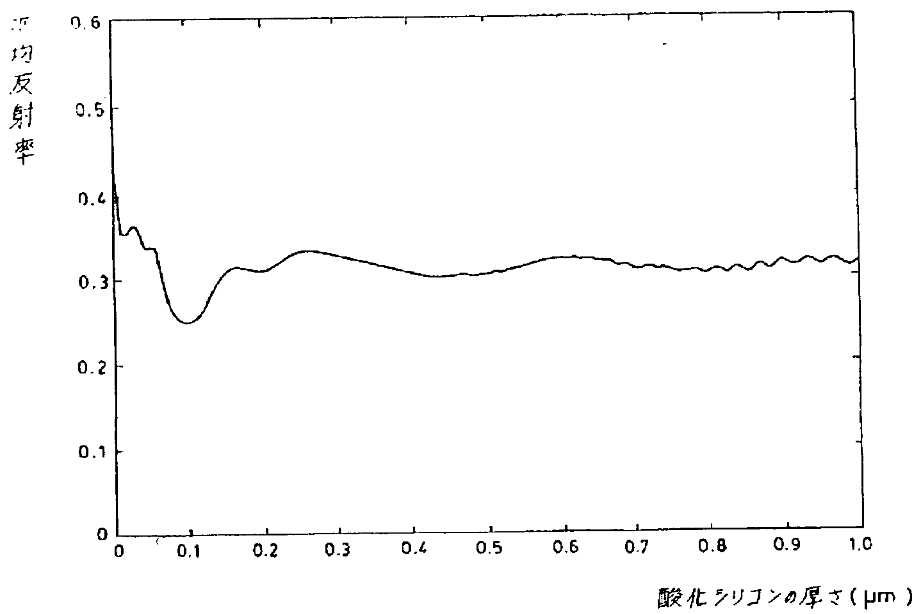

第3図




第4図



第5図


平均反射率
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
酸化シリコンの厚さ(μm)

United States Patent [19]
Arai et al.

[11] Patent Number: 4,525,380
[45] Date of Patent: Jun. 25, 1985

[54] HEATING METHOD OF SEMICONDUCTOR WAFER

[75] Inventors: Tetsuji Arai, Tachikawa; Yoshiki Mimura, Yokohama, both of Japan

[73] Assignee: Ushio Denki Kabushiki Kaisha, Tokyo, Japan

[21] Appl. No.: 582,273

[22] Filed: Feb. 22, 1984

[30] Foreign Application Priority Data

Mar. 16, 1983 [JP] Japan .................................. 58-42204

[51] Int. Cl.³ ................................................ B05D 3/06
[52] U.S. Cl. ...................................... 427/53.1; 427/55
[58] Field of Search .................................. 427/53.1, 55

[56] References Cited

U.S. PATENT DOCUMENTS

4,431,459 2/1984 Teng .................................. 427/53.1

*Primary Examiner*—John H. Newsome
*Attorney, Agent, or Firm*—Ziems, Walter & Shannon

[57] ABSTRACT

A method for heating a semiconductor wafer which may have a first region to be heated and a second region requiring no heating thereof, which method comprises forming a film on a surface of the semiconductor wafer so as to make the reflectivity of the whole surface of the wafer uniform, and then exposing the semiconductor wafer to a flash of light to heat same. The above method permits to heat the whole surface of the wafer at a uniform temperature thereby heating a region of the wafer which is required to be heated, and, at the same time, avoiding any overheating of another region of the wafer where no heating is required. The above heating method is effective for annealing a semiconductor wafer which has large surface area.

4 Claims, 5 Drawing Figures

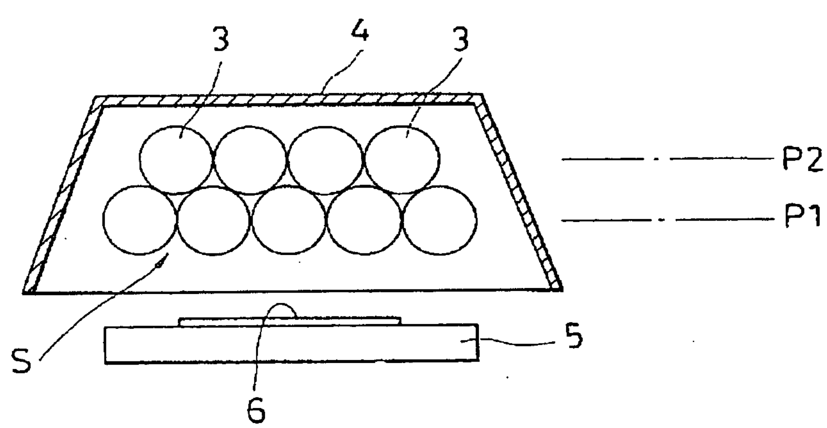


FIG. 1

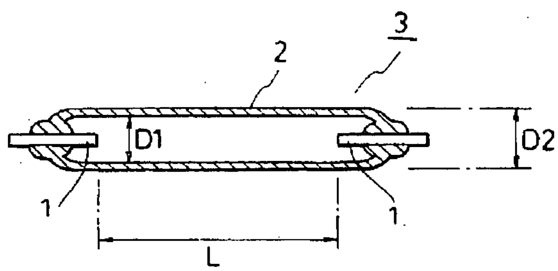



FIG. 2

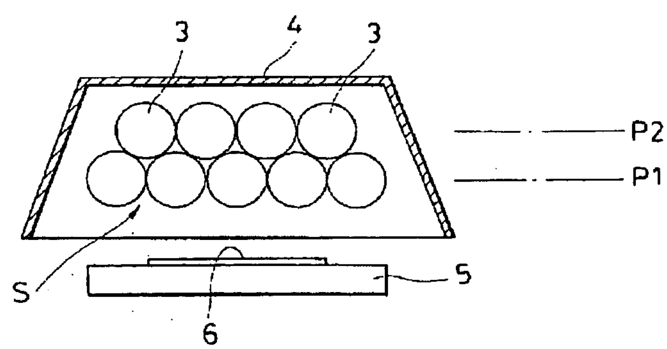


FIG. 3

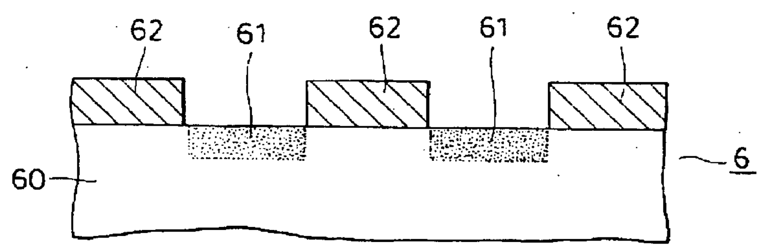



FIG. 4

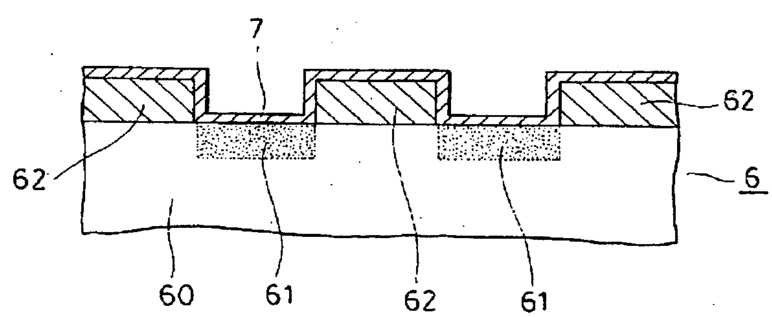
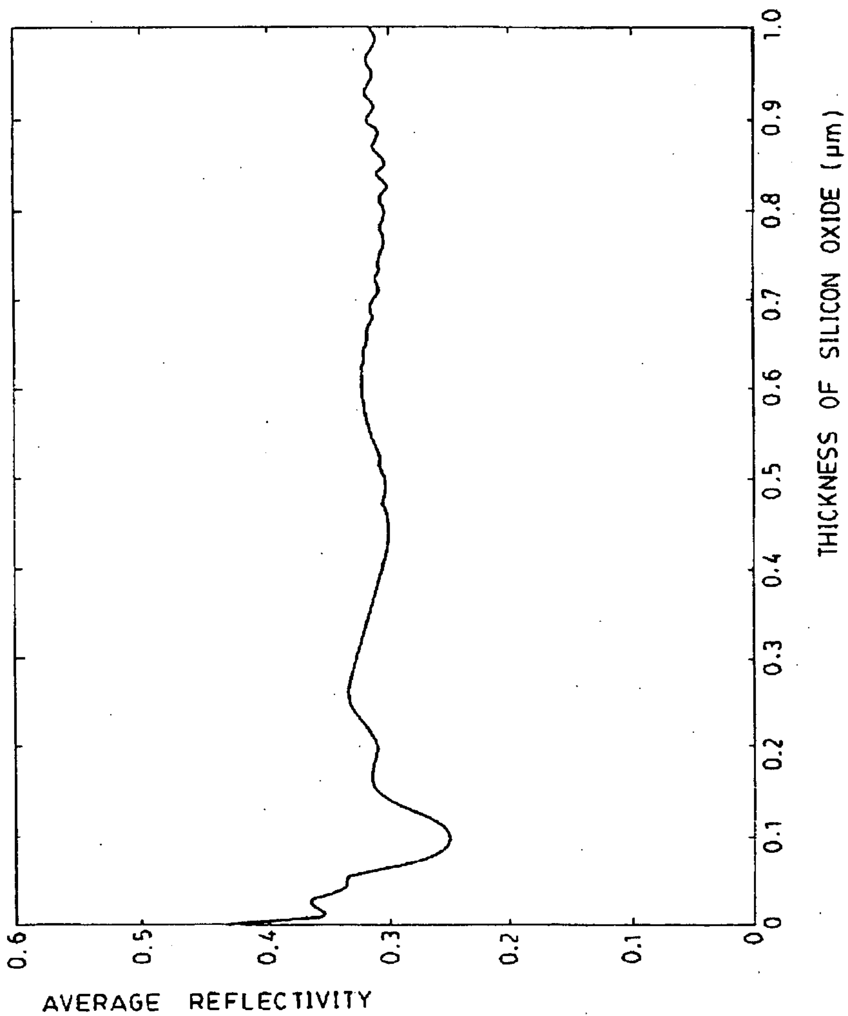


FIG. 5


AVERAGE REFLECTIVITY
0.6
0.5
0.4
0.3
0.2
0.1
0
THICKNESS OF SILICON OXIDE (µm)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0

# HEATING METHOD OF SEMICONDUCTOR WAFER

## BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a heating method of a semiconductor wafer, and more particularly to a heating method of a semiconductor wafer which may have a first region to be heated and a second region requiring no heat thereof and overheating thereof should be avoided.

2. Description of the Prior Art

A semiconductor wafer (hereinafter may be referred to merely as "wafer" for brevity) is used as a substrate for fabricating a semiconductor device such as an integrated circuit or large-scale integrated circuit. In a course of fabrication of such a semiconductor device, a variety of heating steps is required depending on what end use would be made on the semiconductor device. Among such heating steps, there are for example an annealing step for healing crystal defects in an ion-implanted layer of the wafer, a thermal diffusion step for thermally diffusing dopants incorporated in the wafer, a heat treatment step for activating dopants, etc. As a method for conducting, for instance, the annealing step out of the above-mentioned various heating steps, there has conventionally been known to heat a wafer in an electric resistive furnace. Reflecting the recent demand for higher densification of semiconductor devices, it is now required to control a pattern of distribution of dopant atoms along a surface of the wafer more minutely. Thus, it is no longer permissible to ignore thermal diffusion and redistribution of dopant atoms along the surface of the wafer which take place upon annealing each wafer. Owing to the above problem, it is now required to make the annealing time as short as feasible. However, it is difficult to conduct a sufficient heat treatment of a wafer in the electric resistive furnace in a short period of time during which no thermal diffusion of dopant atoms or the like substantially takes place.

With a view toward overcoming the difficulty which electric resistive furnace have encountered, there has been developed a novel annealing method which makes use of laser beam or electron beam. This novel method is certainly effective in carrying out a heat treatment in a short period of time. However, it is accompanied by such problems that damages may occur in a surface of a wafer as the radiant beam is monochromatic having single wavelength and accordingly considerable interference of the radiant beam and reflected beam takes place and a problem of discontinuity or non-uniformity is developed along a boundary of each two adjacent scanning lines when a wafer is scanned by a single beam. Due to such problems, the above annealing method is not suited, especially, for annealing a wafer of large surface area.

With the foregoing in view, it has currently been attempted to develop a method for heating a wafer for annealing by exposing the wafer to a flash of light emitted from flash discharge lamps. Exposing to a flash of light permits to raise the temperature of the wafer to a desired level in a short period of time during which no undesirable problems takes place. In addition, a flash of light, in other words, flashlight is not light of a single wavelength and is thus less susceptible of developing interference of the light, thereby successfully avoiding development of damages in the surface of a wafer. Furthermore, flashlight is not a beam and, corollary to this, does not require to scan the wafer. Therefore, heating process by exposing to flashlight is free of the problem of discontinuity or non-uniformity which is developed along a boundary of each two adjacent scanning lines when the wafer is scanned. Thus, application of a flash of light for annealing a wafer has another merit that the wafer may be of a large surface area.

It is rather rare that a wafer to be subjected to a heat treatment has a uniform reflectivity all over the surface thereof. Generally, a variety of layers such as, for example, an ion-implanted layer, a mask layer made of an oxide film for the ion implantation and the like is formed in a surface of a wafer which is to be heated for its annealing. In a wafer, there are thus a portion which requires heat treatment and a portion which does not require such a heat treatment and should not be overheated, and the former portion (hereinafter called "the first portion") and the latter portion (hereinafter called "the second portion") are generally different in reflectivity. Due to the difference in reflectivity, the final temperature of the first portion is different from that of the second portion no matter how precisely the radiation source, namely, the radiation intensity of each flash of light is controlled. As a result, there is such a problem that the first portion may not always be heated to a desired temperature level and the second portion may, instead, be exposed to undesirable elevated temperature higher than that of the first portion and hence damaged.

## SUMMARY OF THE INVENTION

With the foregoing in view, the present invention has as its object the provision of a heating method of a semiconductor wafer which method permits to achieve a uniform heating of whole surface region of a wafer and to avoid any overheating of any wafer region requiring no heating thereof.

In one aspect of this invention, there is thus provided a method for heating a semiconductor wafer, which method comprises forming a film on a surface of the semiconductor wafer so as to make the reflectivity of the whole surface of the wafer uniform, and then exposing the semiconductor wafer to a flash of light to heat same.

The above heating method permits to uniformly heat the region to be heated and the region requiring no heating thereof thereby necessarily avoiding any overheating of the latter region.

The above and other objects, features and advantages of the present invention will become apparent from the following description and the appended claims, taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a schematic, axial, cross-sectional view of one example of a flash discharge lamp;

FIG. 2 is a simplified, transverse, cross-sectional view of one example of a heating apparatus which is equipped with flash discharge lamps;

FIG. 3 is a fragmentary cross-sectional view of one example of a wafer to be annealed;

FIG. 4 is a fragmentary cross-sectional view of a wafer bearing a film formed on the surface thereof; and

FIG. 5 is a curvilinear diagram showing the relationship between thickness of a film of silicon oxide and average reflectivity thereof.

## DETAILED DESCRIPTION OF THE INVENTION AND PREFERRED EMBODIMENT

One example of this invention will hereinafter be described with reference to the accompanying drawings in which the heating method of this invention is applied to anneal a semiconductor wafer subsequent to its ion implantation.

FIG. 1 illustrates one example of a flash discharge lamp which is used as a light source. Numerals 1, 1 indicate electrodes which are provided in pair. Designated at numeral 2 is a sealed envelope. As exemplary dimensions of the flash discharge lamp, may be mentioned 40 mm, 8 mm and 10 mm respectively as the arc length L, the inner diameter D1 of sealed envelope 2 and the outer diameter D2 of the sealed envelope 2.

FIG. 2 illustrates a heating apparatus constructed by arranging a number of flash discharge lamps each of which has the structure illustrated in FIG. 1. In the illustrated embodiment, nine flash discharge lamps 3 are arranged in two planes P1 and P2 which are parallel to each other and close to each other, namely, five flash discharge lamps 3 and four discharge lamps 3 are arranged close to one another and in a staggered pattern, whereby forming a plane flashlight source S of about 50 mm×40 mm. Numeral 4 indicates a reflector provided surrounding the top and sides of the plane flashlight source S. Designated at numeral 5 is a specimen stage adapted to hold a wafer 6 to be heated at a position about 10 mm underneath the plane flashlight source S. Although not illustrated in the drawing, a heater is provided in a wafer-holding part of the specimen stage 5 so that the wafer 6 can be preheated by the heater prior to carrying out principal heating of the wafer 6 by exposing same to a flash of light.

The wafer 6 may for example be in such a one as depicted in FIG. 3. In FIG. 3, numeral 60 indicates a silicon substrate whereas numeral 62 indicates a mask layer made of silicon oxide provided for implanting ions into desired regions of the silicon substrate 60. Designated at numeral 61 are ion-implanted layers formed by ion-implantation, in which, for example, $5\times10^{15}$ arsenic ions per square centimeter are introduced at 40 KeV into the desired regions of the silicon substrate 60 uncovered with the mask layer 62. The thickness of the silicon substrate 60 is about 300–650 μm. The depth of each of crystal defect-containing portions in the ion-implanted layers 61 is about 0.2–1.0 μm. On the other hand, the thickness of the mask layer 62 is about 0.8 μm. In the wafer 6, regions of the ion-implated layers 61 are regions to be heated and the remaining regions other than the ion-implanted layers 61 are regions requiring no heating thereof.

In one embodiment of this invention, an annealing of the above-described wafer 6 is carried out by heating the wafer 6 in the following manner in the heating apparatus of the above-described structure.

Namely, a film 7 having a thickness of about 0.2 μm and made of silicon oxide is formed first of all over the entire surface of the wafer 6, as shown in FIG. 4. The film 7 may be formed by any thin-film fabrication technique which is known per se in the art.

Next, the wafer 6 bearing the film 7 formed thereon is placed on the wafer-holding part of the specimen stage 5 in the heating apparatus depicted in FIG. 2. Prior to heating the wafer by exposing it to a flash of light, the wafer 6 is preheated to about 350° C. by means of the heater of the specimen stage 5.

When temperature of the wafer 6 has reached about 350° C. due to the heating by the heater, entire surface of the wafer 6 is exposed to a flash of light emitted from the plane flashlight source S so that the entire surface of the wafer 6 are heated. The exposure to a flash of light is carried out under such conditions that the intensity of luminance on the surface of the wafer 6 is 19.8 Joule/cm$^2$ and exposure time (defined as full pulse width at half maximum of the flash of light) is 400 microseconds.

The heating of the wafer 6 is carried out in the manner mentioned above. In a heating of a wafer by exposing it to a flash of light, it is generally known that final temperature of the surface of the wafer can be theoretically derived from conditions of exposing to a flashlight and physical properties of the wafer. Let's now suppose that a wafer is exposed to a flashlight having a full pulse width t (unit: microseconds) at half maximum and a luminance intensity E (unit: Joule/cm$^2$) on the surface of the wafer which has an average reflectivity R. Where the full pulse width t is about 50 microseconds or longer, the final temperature T (°C.) of the surface of the wafer may be expressed approximately by the following equation (1).

$$T = a\cdot(1-R)\cdot E\cdot t^{b} + T_A \tag{1}$$

where,

a,b: constants determined by the thermal conductivity, density, specific heat, etc. of the material making up the wafer;

(1−R)·E: energy per unit area, absorbed in the wafer; and

$T_A$: temperature reached by the preheating of the wafer (if the wafer is preheated).

When the wafer is made of silicon, a and b are respectively about 540 and about −0.37.

The average reflectivity R may be defined by the following equation (2):

$$R = \frac{\int I(\lambda)R(\lambda)d\lambda}{\int I(\lambda)d\lambda} \tag{2}$$

where,

I(λ): intensity of luminance at the wavelength λ; and

R(λ): reflectivity of light of wavelength λ.

In the case of flashlight employed for heating a wafer, I(λ) remains substantially constant. R(λ) is determined by the optical constants (refractive index, attenuation coefficient, etc.) of each wafer or, when a film is formed over the surface of the wafer, by the optical constants (refractive index, attenuation coefficient, etc.) and thickness of the film.

FIG. 5 is a curvilinear diagram showing the relationship between thickness of a film of silicon oxide formed on a surface of a wafer, which is made of silicon, and its average reflectivity R. As apparent from the diagram, the average reflectivity R remains relatively small while the thickness of the film of silicon oxide ranges from about 0.06 μm to about 0.15 μm. When the thickness exceeds 0.15 μm, the average reflectivity R does not vary too much but remains at about 0.31.

Taking the above-described theoretical background into consideration, some calculations will hereinafter be made. In the above-described heating method, the film

7 having a thickness of 0.2 μm and made of silicon oxide is formed on the entire surface of the wafer, then the thickness of silicon oxide film on each region to be heated, namely, each ion-implanted layer 61 of the wafer 6 is 0.2 μm. As determined from the curvilinear diagram of FIG. 5, the reflectivity of the surface of each region to be heated becomes about 0.31. On the other hand, a mask layer 62 is provided over each region which does not require any heating. The mask layer 62 is made of silicon oxide and its thickness is 0.8 μm. Since the film having a thickness of 0.2 μm and made of silicon oxide is further formed over the mask layer 62, the total thickness of silicon oxide on the region is 1.0 μm. As determined in the same manner from the curvilinear diagram of FIG. 5, the reflectivity of the surface of each region requiring no heating thereof also becomes about 0.31. Thus, the reflectivity of the whole surface of the wafer has become uniform. As a result, as readily understood from the above equation (1), the final temperature of the whole surface of the wafer will become uniform. This means that each of the regions, which require to be heated, can be heated desirably and each of the regions, which do not require any heating thereof, are not heated at higher temperature and may be successfully avoided from overheating. Consequently, it is possible to achieve desirable annealing of the wafer and, at the same time, to avoid possible damages of the wafer due to overheating thereof.

Incidentally, the final temperature $T_1$ of the wafer 6 in the above example is calculated in accordance with the equation (1) as follow:

$$T_1 = 540 \times (1-0.31) \times 19.8 \times 400^{-0.37} + 350 = 1154 \text{ (°C.)}$$

Thus, desirable annealing was achieved while successfully avoiding any overheating at each region where no heating is required. Regions which did not require their heating were actually inspected after the heat treatment. No damages were observed there.

As a comparative test, heating was carried out in the same manner as in the above example except that the film 7 was not formed. The ion-implanted layers 61 were thus exposed. The reflectivity of each of the ion-implanted layers 61 was great, namely, 0.43 and the final temperature $T_2$ of each of the region which required their heating was thus calculated as follow:

$$T_2 \times 540 = (1-0.43) \times 19.8 \times 400^{-0.37} + 350 = 1014 \text{ (°C.)}$$

On the other hand, the final temperature $T_3$ of each of the regions where no heating was required was calculated as follow:

$$T_3 = 540 \times (1-0.31) \times 19.8 \times 400^{-0.37} + 350 = 1154 \text{ (°C.)}$$

Namely, the final temperature $T_2$ of each of the regions which required their heating was lower than the final temperature $T_3$ of each of the regions where no heating was required, thereby failing to achieve required annealing.

Furthermore, a further heating test was carried out in the same manner as in the above comparative test except that the plane flashlight source S was adjusted to increase the luminance intensity E to 24 Joule/cm$^2$. The final temperature $T_2$ of each of the regions which required their heating was calculated as follow:

$$T_2 = 540 \times (1-0.43) \times 24 \times 400^{-0.37} + 350 = 1155 \text{ (°C.)}$$

On the other hand, the final temperature $T_3$ of each of the regions where no heating was required was calculated as follow:

$$T_3 = 540 \times (1-0.31) \times 24 \times 400^{-0.37} + 350 = 1324 \text{ (°C.)}$$

Thus, the annealing of each of the ion-implanted layers 61 was successfully achieved but the regions where no heating was required were overheated to considerable extents and developed damages such as additional crystal defects and cracks, whereby making the wafer no longer suitable for actual application.

In the above example, it is also possible to bring about such additional effects as will be mentioned below. In the example, it was employed, as a wafer, the wafer made of silicon and having the mask layer 62 made of silicon oxide, over the regions where no heating was required; as a material making up the film 7, silicon oxide was chosen; the thickness of the film 7 was controlled over 0.15 μm, namely, at 0.2 μm; and the film 7 was formed over the entire surface of the wafer uniformly. As readily envisaged from the curvilinear diagram given in FIG. 5, the reflectivity of the surface of each of the regions which required their heating and reflectivity of each of the regions where no heating was required became uniform. Thus, it is able to make reflectivities of both regions uniform without forming the film 7 selectively on certain specific regions of the wafer, thereby making the formation work of the film 7 extremely easy. Besides, the wafer is preheated prior to heating same by exposing to a flash of light. This permits to lower necessary luminance intensity of the flashlight which is required to raise the temperature of the surface of the wafer to a desired level, thereby prolonging the service life of each flash discharge lamp.

One example of this invention has been described above. It should however be borne in mind that a variety of changes and modifications may be made in the present invention. For example, it may be feasible to employ, as a material making up the film 7, silicon nitride ($Si_3N_4$ or the like), PSG ($SiO_2$ glass containing 8% of $P_2O_5$), alminum or the like instead of silicon oxide. Similar to the film of silicon oxide, reflectivity of a film made of such material can be made uniform by selecting the thickness of the film. The film 7 may be formed only over regions which are required to be heated or only over regions where no heating is required. Alternatively, the film 7 may also be applied to different thicknesses over regions which are required to be heated and regions where no heating is required. It is necessary to make the reflectivity of the surface of each region, which is to be heated and the reflectivity of the surface of each region where no heating is required, uniform by the provision of the film 7, no matter how the film 7 is applied.

In the above example of this invention, the ion-implanted layers of the wafer were annealed. Needless to say, the present invention may also be applied to other heat treatment of a wafer.

Having now fully described the invention, it will be apparent to one of ordinary skill in the art that many changes and modifications can be made thereto without

departing from the spirit or scope of the invention as set forth herein.

What is claimed is.

1. A method for heating a semiconductor wafer comprising:

forming a film on an entire surface of the semiconductor wafer so as to make the reflectivity of said entire surface of the wafer uniform,

and heating said entire surface by exposing said entire surface to a flash of light at one time.

2. A method as claimed in claim 1, wherein the step of forming a film comprises forming on said surface of the semiconductor wafer a silicon oxide film having a thickness greater than 0.15 $\mu m$.

3. A method for heating a semiconductor wafer comprising:

forming a film on an entire surface of the semiconductor wafer so as to make the reflectivity of said entire surface of the semiconductor wafer uniform;

disposing the semiconductor wafer in a heating apparatus, which comprises a plurality of flash discharge lamps arranged close to one another so as to define a plane flashlight source, in a position such that said surface of the semiconductor wafer faces the plane flashlight source; and

operating the heating apparatus to expose said entire surface of the semiconductor wafer at a time to a flash of light emitted from the plane flashlight source to heat said entire surface.

4. A method as claimed in claim 3, wherein the step of forming a film comprises forming on said surface of the semiconductor wafer a silicon oxide film having a thickness greater than 0.15 $\mu m$.

* * * * *